REMARKS

Filed concurrently herewith is a Request for a One-Month Extension of Time which extends the shortened statutory period for response to February 18, 2006. Accordingly, Applicant respectfully submits that this response is being timely filed.

The Official Action dated October 18, 2005 has been received and its contents carefully noted. In view thereof, claims 1-4 have been amended and new claims 5-9 have been added in order to better define that which Applicant regards as the invention. Accordingly, claims 1-9 are presently pending in the instant application.

Initially, Applicant wishes to acknowledge the Examiner's indication in paragraph 5 of the Office Action that claims 2 and 4 have been objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. With the foregoing amendments, it is respectfully submitted that independent claim 1 distinguishes over the prior art of record and is in proper condition for allowance. Therefore, it is respectfully requested that all claims of the present application be indicated as being allowable over the prior art of record but certainly it is respectfully requested that claims 2 and 4 again be indicated as being allowable over the prior art of record.

Turning to page 2 of the Office Action, claims 1 and 3 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,764,899 issued to Lewallen et al. This rejection is respectfully traversed in that the patent to Lewallen et al. neither discloses nor suggests that which is presently set forth by Applicant's claimed invention.

As can be seen from the foregoing amendments, independent claim 1 has been amended to recite a multi-port semiconductor memory comprising a memory cell array including a plurality of memory cells, a first bit line pair performing write-in or read-out of

complementary date for said memory cells in said memory cell array, a second bit line pair performing write-in or read-out of complementary data for said memory cells in said memory cell array, a plurality of first word lines provided to each of said memory cells for selecting a first memory cell from said memory cell array, a plurality of second word lines provide to each of said memory cells for selecting a second memory cell from said memory cell array, and a first pull-up circuit that, when data is written in said first memory cell from said first bit line pair, pulls up low-level of a lower-level line in said first bit line pair. Particularly as the Examiner can readily appreciate, the present invention as set forth in amended claim 1 includes a first pull-up circuit which pulls up low-level of a lower-level line in the first bit line pair when data is written in the first memory cell from the first bit line pair. The multi-port semiconductor memory of the present invention can pull up the low-level of the data written in the memory cell. Accordingly, since potential difference between a low-level bit line and a high-level bit line becomes small, the coupling noise is suppressed. Further, as noted in Applicant's specification at page 4, lines 5-9, a multi-port semiconductor memory in which the wrong read-out is rarely generated and operation speed is substantially fast is obtained. Clearly, the patent to Lewallen et al. neither discloses nor remotely suggests these features.

Specifically, it is noted that Lewallen et al. states in column 4, lines 27-30 that "when pass gates 11-17 and 23, 25, 29, and 31 are in a no-pass condition, the potentials on all four bit lines are maintained at approximately a logic level by four bit line leaker gates 39, 41, 43 and 44." Further, Lewallen et al. goes on to state at lines 34-37 of column 4, that "consequently, when all the pass gates are in a no-pass condition, leakers 39-45 will cause the potential on each bit line to rise to nearly a logic 1 level." That is, the potential level of bit lines is pulled up to a logic 1 level when data is not written in in accordance with the

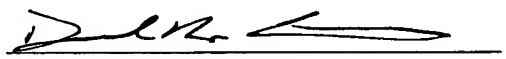
teachings of Lewallen et al. Clearly, Lewallen et al. does not disclose or suggest that a first pull up circuit pulls up low-level of a lower level line in the first bit line pair when data is written in the first memory cell from the first bit line pair as is specifically recited by Applicant's claimed invention. Accordingly, it is respectfully submitted that independent claim 1 as well as those claims which depend therefrom clearly distinguish over the teachings of Lewallen et al. and are in proper condition for allowance.

With respect to new claims 5-9, each of these claims are either directly or indirectly dependent upon independent claim 1 and include all the limitations thereof. Accordingly, it is respectfully submitted that each of these claims are likewise in proper condition for allowance.

Therefore, in view of the foregoing it is respectfully requested that the objections and rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-9 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,



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